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DESIGN OF MULTILEVEL INVERTER WITH LESS NUMBER OF POWER ELECTRONIC COMPONENTS FED TO INDUCTION MOTOR

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ABSTRACT

Multilevel inverters which have a high number of components. This is a subject of increasing importance I high-power inverters. Advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability. The main disadvantages of this technique are that a larger number of switching semiconductors are required for lower-voltage systems and the small voltage steps must be supplied on the dc side either by a capacitor bank or isolated voltage sources. The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. The analytical analyses of the power losses of the proposed converter are also presented. The operation and performance of the proposed multilevel converter have been evaluated with the experimental results of a single-phase 125-level prototype converter.

KEYWORDS: CHB, Multilevel Converter, Cascaded Multilevel Converter, Full-Bridge Converter, Bidirectional Switch

INTRODUCTION

ML inverters are an array of power semiconductors and capacitors that allow for the generation of a high-quality load voltage. Today, the three most popular and widely used families of ML inverters in industry are neutral point (NP) clamped (NPC), flying capacitor (FC), and CM [2], [3]. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. Numerous multilevel converter topologies and wide variety of control methods have been developed in the recent literature [1]–[4]. Three different basic multilevel converter topologies are the neutral point clamped (NPC) or diode clamped [1], the flying capacitor (FC) or capacitor clamped [6] and the cascaded H-bridge (CHB) [7]. The main drawbacks of NPC topology are their unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing and requiring a great number of clamping diodes for higher level. The FC multilevel converter uses flying capacitor as clamping devices. These topologies have several attractive properties in comparison with the NPC converter, including the advantage of the transformer less operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches [8], [9]. But, these converters require an excessive number of storage capacitors for higher voltage steps. The CHB topologies are proper option for high level applications from point of view of modularity and simplicity of control. But, in this topology, a large number of isolated dc voltage sources are required to supply each conversion cell. It increases the converter cost and complexity In multilevel converter, the power quality is improved as the number of levels increases at the output voltage.

However, it causes to the increasing number of switching devices and other components, and increases the cost and control complexity and tends to reduce the overall reliability and efficiency of the converter. These converters reduce the size and cost of the converter and improve the reliability since fewer semiconductors and capacitors are employed [5].

The hybrid multilevel converters are composed of different multilevel topologies with unequal values of dc voltage sources and different modulation techniques and/or semiconductor technologies [8]. With appropriate selection of switching devices, the converter cost is significantly reduced. But, the application of different multilevel topologies result in loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [6]. By the presented algorithm in [10] and [11], it is not possible to create all levels (odd and even) at the output voltage, and it reduces the flexibility of the converter. Also, to create the output voltage with a constant number of levels, the converter needs many large numbers of bidirectional switches. To overcome these disadvantages, [9] has presented a new topology, which has decreased the number of bidirectional switches and dc voltage source compared with the ability of the production of all levels at the output voltage. The main drawback of this topology is the utilization of unidirectional switches that operate in the high output voltage. These structures provide a high number of output levels using low number of components. But, the main drawback of these topologies is the utilization a full-bridge converter, which operates in the high output voltage. This paper proposes a new modular and simple topology for cascaded multilevel converter that produces a high number of levels with the application of a low number of power electronic components. Then, a procedure for calculating the values of required dc voltage sources is also proposed. In addition, the structure of the proposed topology is optimized for various aims. Finally, a design example of the proposed multilevel converter is included.

MULTILEVEL CONVERTER WITH REDUCED NUMBER OF SWITCHES

The basic unit of the sub-multilevel converter, is illustrated in Figure 1. It consists of several capacitors (with dc voltages) and bidirectional switches. If *n* capacitors are used, *n* + 1 different values can be obtained for *vo*, by *n* + 1 bidirectional switches. The output voltage of this sub-multilevel converter has zero or positive values.

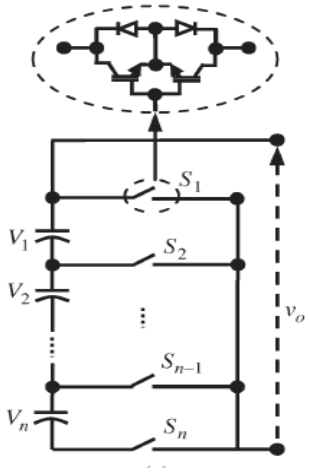


Figure 1: Basic Unit of the Sub Multilevel Converter

The presented unit requires bidirectional switches with the capability of blocking voltage and conducting current in both directions. Several arrangements can be used to create bidirectional switches considering of insulated gate bipolar transistors (IGBTs) and diodes. The proper configuration of bidirectional switches is arranged by a common emitter connection of two IGBTs, which each one of IGBTs has an anti parallel diode. Because the emitters of two IGBTs are common, the base voltage of each IGBT can be measured versus its common emitter. Therefore, a bidirectional switch requires a gate driver circuit in this configuration. This configuration of bidirectional switch is used in this paper. The cascaded connection of these sub-multilevel converters increases the possible value of *vo*, effectively. But, it can only generate the positive output voltages. To generate both positive and negative voltages, a full-bridge converter is connected to the output terminal of the cascaded connection of sub-multilevel converters. But, the unidirectional switches in the

full-bridge converter and some bidirectional switches, such as *S*1, must operate at the high output voltage and need higher voltage blocking.

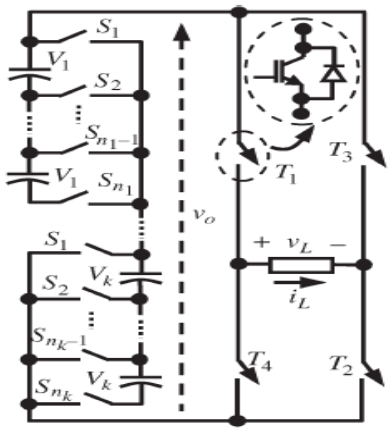


Figure 2: Sub Multilevel Converters in Series

As a result, the cost and losses will be increased and its industrial applications will be limited. Figure 2 shows *k* sub-multilevel converters in series, where the structure of the first till *k*th sub-multilevel converters has *n*1, *n*2, . . . , *nk* bidirectional switches, respectively. In this case, only one switch of each sub-multilevel converter turns on in different operation modes of the converter. The number of output voltage levels (*N-level*) and IGBTs (*NIGBT*) are given by the following equations, respectively.

$$N_{level}=2\left(\prod_{i=1}^{k} n_i\right)-1=2(n_1\times n_2\times\ldots\times n_k)-1 \tag{1}$$

$$N_{IGBT}=2\left(\sum_{i=1}^{k} n_i\right)+4=2(n_1+n_2+\ldots+n_k)+4. \tag{2}$$

The maximum value of the output voltage (*Vo*max) can be obtained, as follows

$$V_{o\max}=\sum_{i=1}^{k}(n_i-1)V_i. \tag{3}$$

PROPOSED TOPOLOGY

The proposed topology for a sub-multilevel converter, hereafter called multilevel module (MLM), which is used for the implementation of the proposed multilevel converter topology. It consists of *n* dc voltage sources and *n* bidirectional switches. A MLM produces a staircase voltage waveform with positive polarity. It is connected to a single phase full-bridge converter, which particularly alternates the input voltage polarity and provides positive or negative staircase waveform at the output. The full-bridge converter has four unidirectional switches, which consists of an IGBT and an antiparallel fast recovery diode.

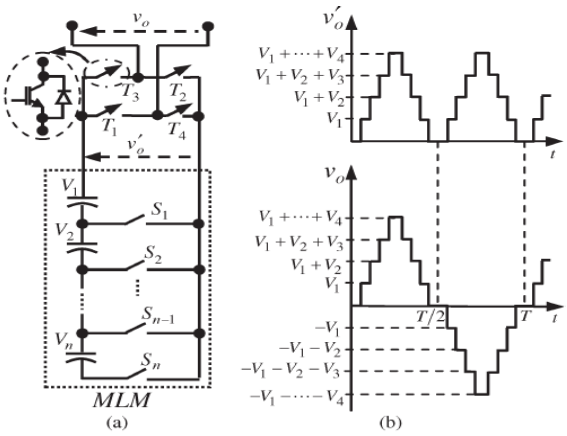


Figure 3: (a) Proposed Sub Multilevel Topology and (b) Typical Output Waveform of *vo*

The typical output waveform of v^1o and *vo* are shown in Figure 3(b). It is noticeable that only one switch turns on in different operation modes of the MLM and also, both switches *T*1 and *T*4 (or *T*2 and *T*3) cannot be simultaneously turned on because of a short circuit occurrence across dc voltage sources and then the voltage *vo* would be produced. For simplicity, the on state voltage drops of switches have been neglected. As it can be seen, 2*n* + 1 different value can be obtained for *vo*.

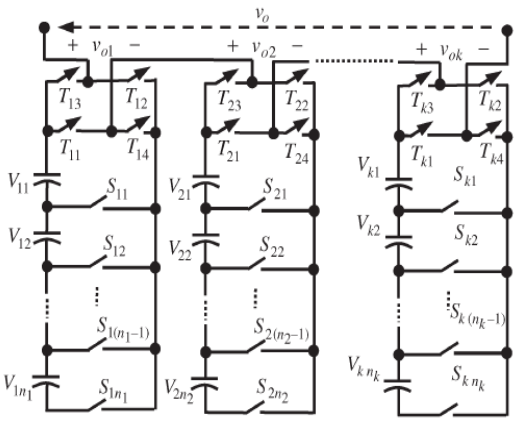


Figure 4: Proposed Multilevel Converter Topology

The proposed multilevel converter topology, which is based on the combination of MLMs and full-bridges converters, is shown in Figure 4. The structure of the first till *k*th MLM has *n*1, *n*2, . . . , *nk* bidirectional switches, respectively. Each MLM can generate a stepped voltage waveform with positive polarity.

The full-bridge converters provide positive and negative stepped voltage waveforms in their output. The different output voltage levels can be determined by the combination of switching states of MLMs. It is obvious that only one switch of each MLM turns on in different operation modes of the converter without considering the zero voltage state of MLMs. It should be noted that the capacitors can be replaced with the dc voltage sources in the proposed topology. Although this topology requires multiple dc voltage sources, but they may be available in some systems through renewable energy sources, such as photovoltaic panels or fuel cells, or with energy storage devices, such as capacitors or batteries. When ac voltage is already available, then, multiple dc sources can be generated using isolated transformers and rectifiers. If the voltage sources are changed during the converter operation, the voltage balancing should be done. For example, the output voltages of fuel cells are variable. Therefore, if they are used at dc-link, the quality of output voltage of the converter will

be reduced. The hardware proposed method to dc-link balancing is shown in Figure 4. The capacitor voltages are controlled with the DC/DC converters.

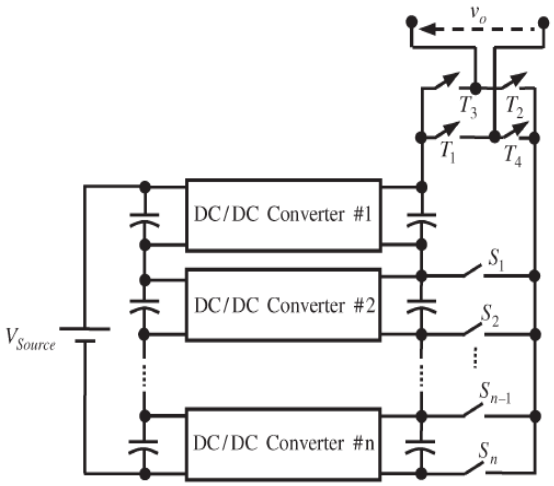


Figure 5: DC-Link Voltage Balancing

From figure 5 we getting the equations represented below

The number of output voltage levels can be determined by the following equation

$$N_{level} = \prod_{i=1}^{k}(2n_i + 1)$$
$$= (2n_1 + 1) \times (2n_2 + 1) \times \ldots \times (2n_k + 1) \quad (4)$$

Considering the selected common emitter configuration for bidirectional switches, the number of power IGBTs in the proposed topology can be obtained as follows

$$N_{IGBT} = 2(n_1 + n_2 + \ldots + n_k) + 4k \quad (5)$$

It is important to note that the number of IGBTs and main diodes are the same

OPTIMAL STRUCTURES

Maximum Number of Voltage Levels with Constant Number of IGBTs

To maximize the number of levels using the minimum number of IGBTs is the motto of the desirable object in a multilevel converter. The question is which topology can provide a maximum number of output voltage levels concerning the proposed structure is that for the constant number of IGBTs, The product of numbers, whose summation is constant, will be maximum, when all are equal. Then considering (4) and (5) we have

$$n_1 = n_2 = \ldots = n_k = n. \quad (6)$$

Using (5) and (6), we have

$$k = \frac{N_{IGBT}}{2n + 4}. \quad (7)$$

Now, the value of n must be determined. Considering (4) and (6), the maximum number of voltage levels will be determined

$$N_{level} = (2n+1)^k \tag{8}$$

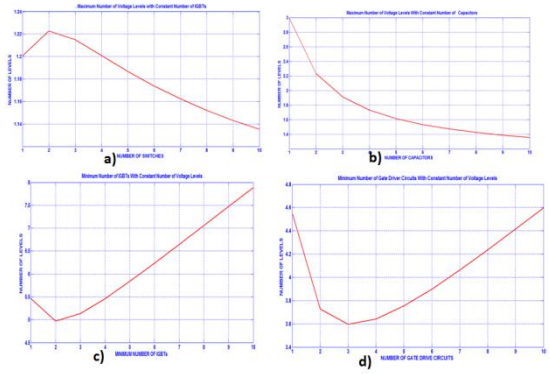


Figure 6: (a) Variation of (2n + 1)1/(2n+4), (b) (2n + 1)1/n, (c) (2n +4)/ ln(2n + 1) and (d) (n + 4)/ ln(2n + 1) versus n.

Considering (7) and (18), we have

$$N_{level} = \left[(2n+1)^{1/(2n+4)}\right]^{N_{IGBT}} \tag{9}$$

The variation of (2n + 1)1/(2n+4) versus n is shown in Figure 6(a). It is clear that the maximum number of voltage levels is obtained for n = 2. Thus, a structure consisting of two bidirectional switches (i.e., two dc voltage sources) in each MLM can provide the maximum voltage levels for v_o with using minimum numbers of IGBTs. It is necessary to notice that the number of components is an integer. Thus, if an integer number is not obtained, the nearest integer number should be selected.

Maximum Number of Voltage Levels with Constant Number of Capacitors

Imagine the number of capacitors (dc voltage sources) is constant and equal to (N capacitor), in this section the question is which topology provides the maximum number of voltage levels. Suppose the proposed topology consists of a series of k MLMs and each of them consists of ni capacitors (i =1, 2, . . . , k). Thus

$$N_{capacitor} = \sum_{i=1}^{k} n_i = n_1 + n_2 + \ldots + n_k. \tag{10}$$

Considering (16), the number of capacitors can be written as follows:

$$N_{capacitor} = n \times k \tag{11}$$

Using (8), the maximum number of voltage levels can be Determined

$$N_{level} = \left[(2n+1)^{1/n}\right]^{N_{capacitor}} \tag{12}$$

Figure 6 shows the variation of (2n + 1)1/n versus n. It is clear that the maximum number of voltage levels is obtained for n = 1. Thus, a structure consisting of MLMs with one capacitor (dc voltage source) can provide maximum voltage levels for v_o with minimum numbers of capacitors. It is necessary to note that the proposed topology is converted in this case to the conventional cascaded multilevel converter.

Number of IGBTs with Constant Number of Voltage Levels

In the following section, the question that arises is that if N level is the number of voltage levels considered for the voltage vo, which topology with a minimum number of IGBTs can produce it? It can be proven that the maximum number of voltage levels may be obtained for equal bidirectional switches. Thus, if the number of switches in each MLM is assumed to be equal to n, then the total numbers of IGBTs (NIGBT) can be obtained, considering (15) and (18), as follows:

$$N_{IGBT} = (2n+4)k = \ln(N_{level}) \times \frac{(2n+4)}{\ln(2n+1)}. \tag{13}$$

Since N level is constant, NIGBT will be minimized, when (2n + 4)/ ln(2n + 1) tends to be minimum. Figure 6(c) shows that the minimum number of IGBTs to realize N level values for the output voltage is possible for n = 2.

Minimum Number of Gate Driver Circuits With Constant Number of Voltage Levels

In the suggested topology, each bi directional switch consists of two IGBTs and two anti-parallel diodes. Also, there is a composition of an IGBT and an anti-parallel diode each unidirectional switch used in full-bridge converter. Each bidirectional and unidirectional switch in the converter requires an isolated driver circuit. The isolation can be provided using either pulse transformers or opto isolators. The opto isolators can work in a wide range of input signal pulse widths, but a separate isolated power supply is required for each switching device. To reduce the number of components, the objective is to determine the topology, which can provide vo with the minimum number of gate driver circuits. If the number of switches in each MLM is assumed to be equal to n, then, the total numbers of gate drive circuits (N driver) can be obtained, as follows:

$$N_{driver} = (n+4)k = \ln(N_{level}) \times \frac{(n+4)}{\ln(2n+1)}. \tag{14}$$

Since N level is constant, N driver will be minimized, when (n + 4)/ ln(2n + 1) tends to be minimum. Figure 6(d) shows that the minimum number of gate drive circuits to realize N step values for voltage vo is realizable for n = 3

Minimum Blocking Voltage of Switches with Constant Number of Voltage Levels

There is a vital role in the voltage and current ratings of switches in a multilevel converter in the cost and realization of multilevel converters. In all topologies, currents of all switches are equal to the rated current of the load. But, this is not the case for the voltage. The major aim is to determine the topology with the minimum blocking voltage, which can provide constant number of voltage levels vo. Suppose the peak value of the blocking voltage of switches (V switch) is represented by the following equation:

$$\begin{aligned} V_{switch} &= V_{switch,M} + V_{switch,B} \\ &= \sum_{j=1}^{k} V_{switch,m,j} + \sum_{j=1}^{k} V_{switch,b,j}. \end{aligned} \tag{15}$$

In this equation, V switch, M and V switch, B are the peak values of the blocking voltage of the bidirectional and unidirectional switches, respectively. Also, V switch, m, j and V switch, b, j represent the peak value of the blocking voltage of bidirectional switches in the jth MLM and unidirectional switches in the jth full-bridge converter, respectively. Therefore, (15) can be considered as a criterion to compare different topologies from the viewpoint of the maximum

voltage on the switches. The lower value of the criterion indicates that a smaller voltage is applied to the terminal of the switches. According to Figure 6, the following equations can be obtained:

$$V_{switch,m,j} = P \times V_j, \quad j = 1, \ldots, k. \tag{16}$$

Therefore, the peak value of the blocking voltage of MLM switches can be written, as follows:

$$V_{switch,M} = P \times (V_{11} + V_{21} + \ldots + V_{k1}) \tag{17}$$

In these equations, P is calculated by the following equation:

$$\begin{aligned} P &= 2\left[(n-1) + (n-2) + \ldots + \left(n - \frac{n-2}{2}\right)\right] + \frac{n}{2} \\ &= \frac{3n^2}{4} \qquad (\text{if } n \text{ is an even number}) \\ P &= 2\left[(n-1) + (n-2) + \ldots + \left(n - \frac{n-1}{2}\right)\right] + n \\ &= \frac{3n^2+1}{4} \qquad (\text{if } n \text{ is an odd number}). \end{aligned} \tag{18}$$

From above equations

$$\begin{aligned} V_{switch,M} &= P \times \left[1 + (2n+1) + \ldots + (2n+1)^{k-1}\right] \\ &= \frac{P}{2n} \times (N_{level} - 1) \times V_{dc}. \end{aligned} \tag{19}$$

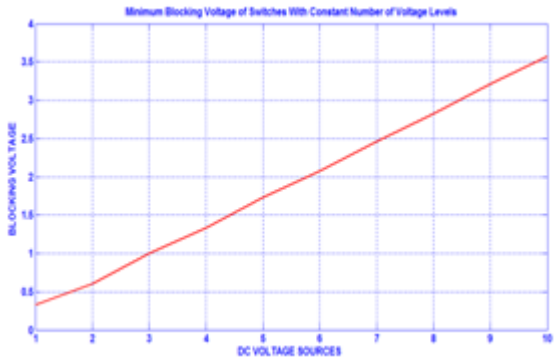


Figure 6(e): Variation of (P/2n) + 1 Voltage versus n

The peak value of the blocking voltage of switches in the jth full-bridge converters can be calculated, as follows:

$$V_{switch,b,j} = 2 \times \sum_{i=1}^{n} V_{ji} = 2n \times (2n+1)^{j-1} \times V_{dc}. \tag{20}$$

The peak value of the blocking voltage of full-bridges switches (Vswitch,B) can be calculated, as follows:

$$\begin{aligned} V_{switch,B} &= \sum_{j=1}^{k} V_{switch,b,j} = V_{dc} \times \left[(2n+1)^k - 1\right] \\ &= V_{dc} \times (N_{level} - 1). \end{aligned} \tag{21}$$

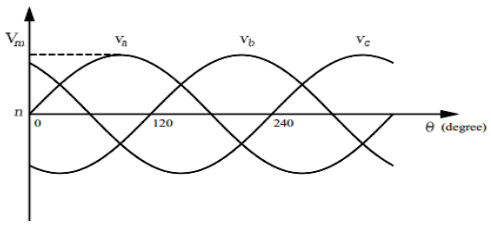
Therefore, the peak value of the blocking voltage of all switches can be written, as follows:

$$V_{switch} = V_{switch,M} + V_{switch,B} = V_{dc} \times \left(\frac{P}{2n} + 1\right) \times (N_{level} - 1). \quad (22)$$

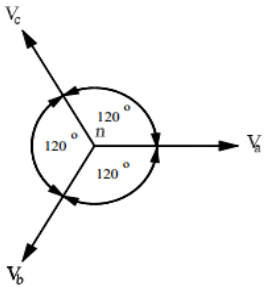
The variation of P/2n + 1 versus n is shown in Figure 6. As illustrated in this Figure, Vswitch is minimum for n = 1. Thus, the optimal structure, from the point of view of the minimum blocking voltage of switches, is a classic full-bridge cell with one dc voltage source and in this case, the proposed topology is converted to the conventional cascaded multilevel converter. Here, the dc voltage sources of H-bridges have been scaled by the factor of three.

SINGLE PHASE TO 3-PHASE INDUCTION MOTOR

The 3-phases induction motor might be used for powerful more than single-phase induction motor, because it can be given the high power when comparison with single phase induction motor as the same size. But the three phase induction motor must be connected to the three phase supply which have phase voltage waveform are difference and phasor diagram that shown in Figure 7(a),(b) and can be written in the equation (1) .



(a) Three-Phases Voltage Waveform



(b) Phasor Diagram

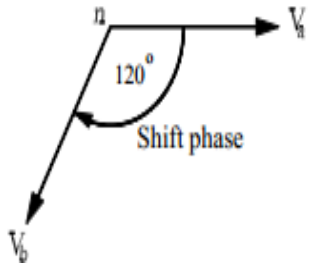
Figure 7: Three-Phase Voltage Waveform and Phasor Diagram

$$v_a = V_m \sin(\omega t + 0°)$$
$$v_b = V_m \sin(\omega t - 120°)$$
$$v_c = V_m \sin(\omega t + 120°) \quad (23)$$

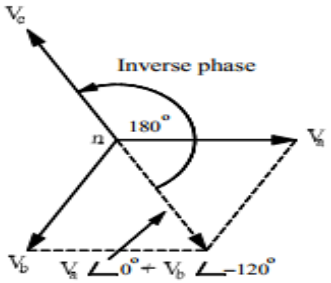
So that, if you want to drive three-phase induction motor by using single-phase waveform, you must be shift the phase voltage into two-phase waveform by connect a capacitor that shown in Figure 2 with this connection, its look like split phase induction motor, the motor will continue turning on the single phase supply but the performance of a motor is fairy poor.

Single Phase to Three Phase Converter

Figure 8 is the concept for convert single phase to three phases sinusoidal waveform; start from phase voltage V_a is shift to 120°lagging for generated phase voltage V_b. After that summing V_a, V_b together and inverse phase for generated phase voltage V_c.



(a) Phase Voltage V_b



(b) Phase Voltage V_c

Figure 8: Single-Phase Voltage Converts to Three-Phase Voltage

DESIGN OF MULTILEVEL CONVERTER BASED ON PROPOSED TOPOLOGY

The optimal multilevel structure is presented in Figure 9(a) for the minimum number of used switches. As shown in this figure, the number of IGBTs and capacitors are 24 and 6, respectively. In this design, the number of voltage levels is 125. The optimal structure based on the minimum number of capacitors is similar to Figure 9(a). The optimal structure based on the minimum number of gate driver circuits is shown in Figure 9(b). In this structure, the number of gate driver circuits is 21 and the number of voltage levels is 343.

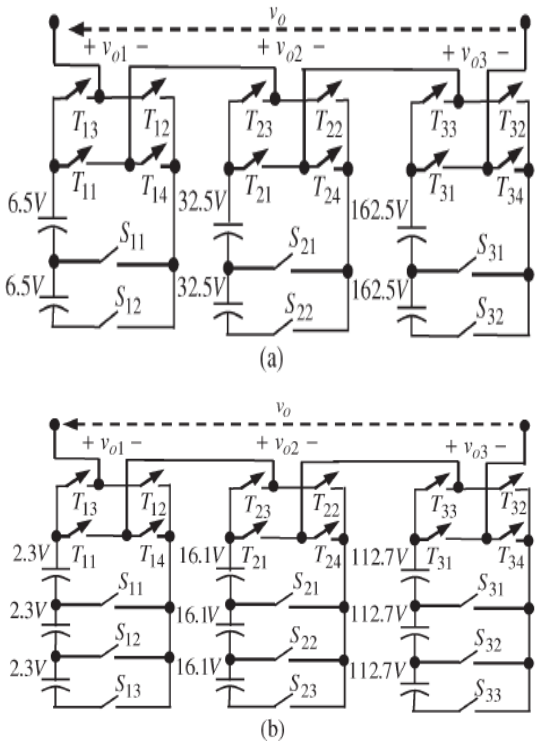


Figure 9: Optimal Multilevel Structure with Minimum Used (a) Switches (b) Gate Driver Circuits

A typical single-phase multilevel converter with a minimum of 120 voltage levels and a peak value of 400V should be designed in above figure.

MATLAB MODELING AND SIMULATION RESULTS

Here simulation is carried out in different cases with respect to reduced components, 1). Proposed 13 level Multilevel Inverter Applied to Induction Machine Drive. 2). Proposed 25 level Multilevel Inverter Applied to Induction Machine Drive. 3). Proposed 35 level Multilevel Inverter Applied to Induction Machine Drive

Case 1: Proposed 13 level Multilevel Inverter Applied to Induction Machine Drive

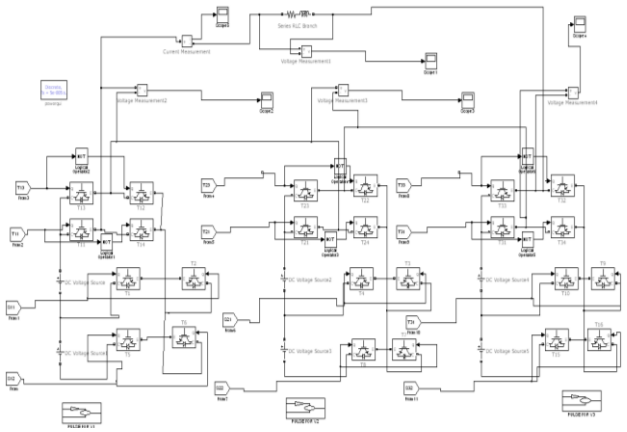


Figure 10: Matlab/Simulink Model of Proposed 13 Level Multilevel Inverter Applied to Induction Machine Drive

Figure 10 shows the Matlab/Simulink Model of Proposed 13 level Multilevel Inverter Applied to Induction Machine Drive using Matlab/Simulink platform.

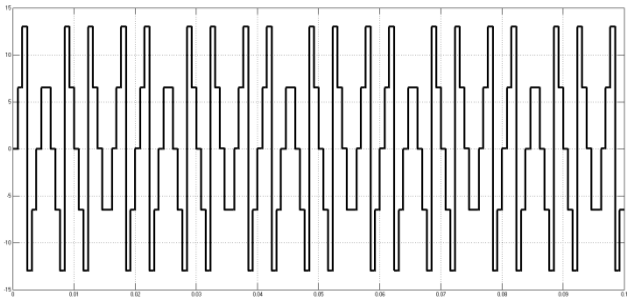


Figure 11: Output Voltage of First Full Bridge

Figure 11 shows the Output Voltage of First Full Bridge Converter.

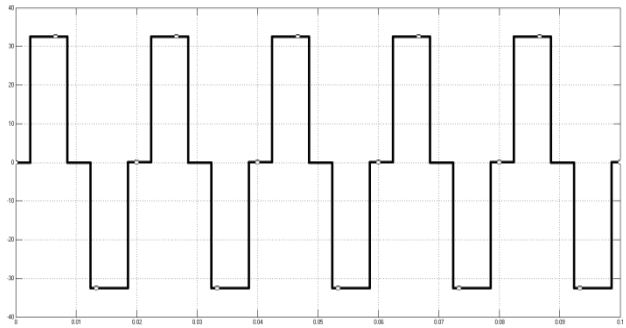


Figure 12: Output Voltage of Second Full Bridge

Figure 12 shows the Output Voltage of Second Full Bridge Converter.

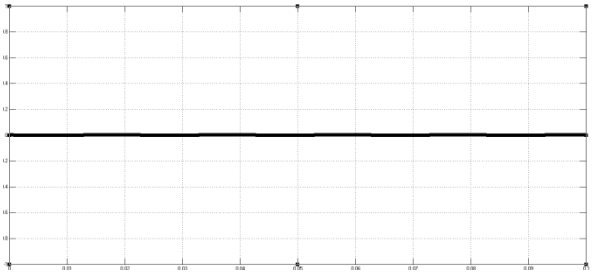


Figure 13: Output Voltage of Second Full Bridge

Figure 13 shows the Output Voltage of Second Full Bridge Converter.

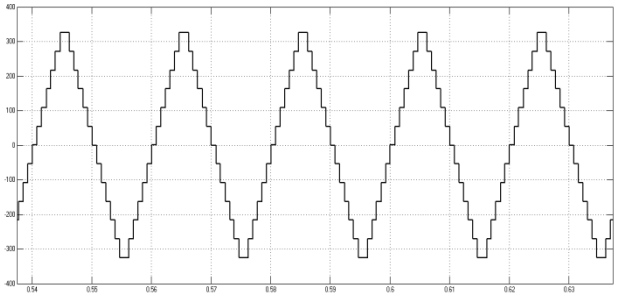


Figure 14: Output Voltage Wave form of 13 Level Inverter

Figure 14 shows the Output Voltage Proposed 13 level Multilevel Inverter.

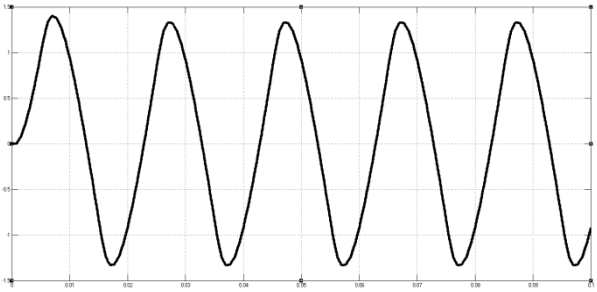


Figure 15: Converter Current

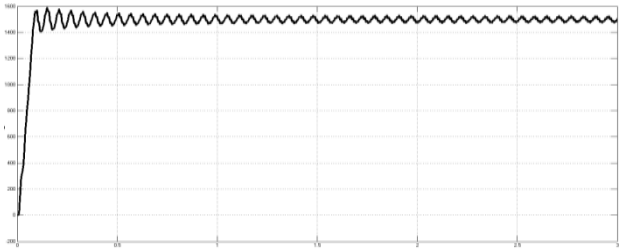


**Figure 16: Speed Characteristics of Induction Fed Motor by 13 Level Inverter **

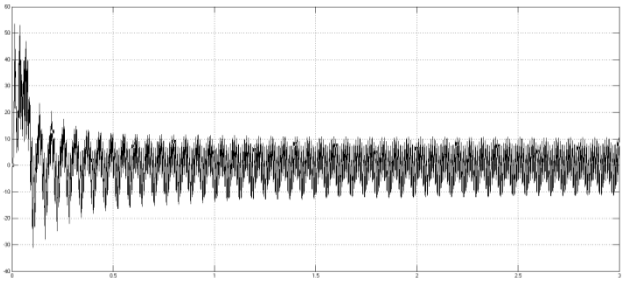


Figure 17: Toque Characteristics of Induction Fed Motor by 13 Level Inverter

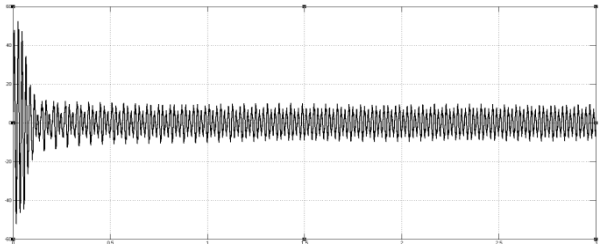


Figure 18: Stator Characteristics of Induction Fed Motor by 13 Level Inverter

As above Figure 16, 17, 18 shows the Speed, Electromagnetic Torque, Stator Current of Proposed 13 level Inverter Fed Induction Motor Drive.

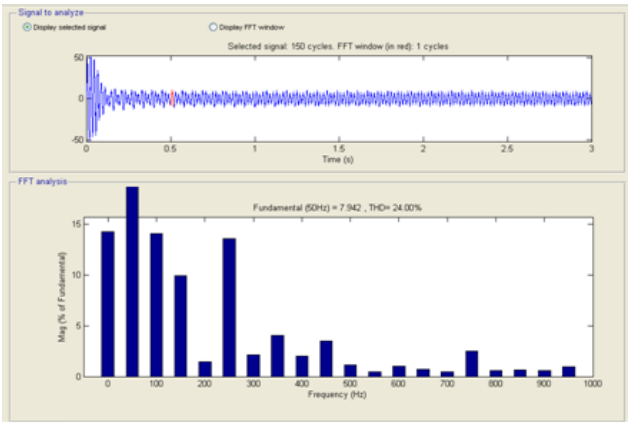


Figure 19: FFT Analysis of Stator Currents of Induction Fed Motor by 13 Level Inverter

Figure 19 shows the FFT analysis of Stator currents of Induction fed motor by 13 Level Inverter, we get THD as 24%.

Case 2: Proposed 25 level Multilevel Inverter Applied to Induction

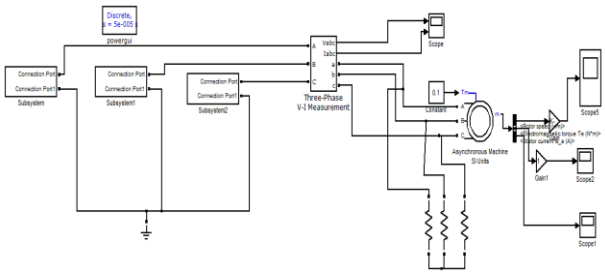


Figure 20: Matlab/Simulink Model of Proposed 13 Level Multilevel Inverter Applied to Induction Machine Drive

Figure 20 shows the Matlab/Simulink Model of Proposed 13 level Multilevel Inverter Applied to Induction Machine Drive using Matlab/Simulink platform.

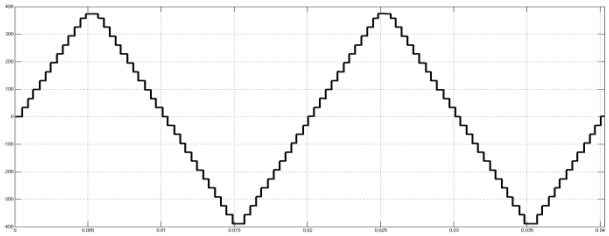


Figure 21: Output Voltage Wave form of 25 Level Inverter

Figure 21 shows the Output Voltage of Proposed 25 level Multilevel Inverter Applied to Induction

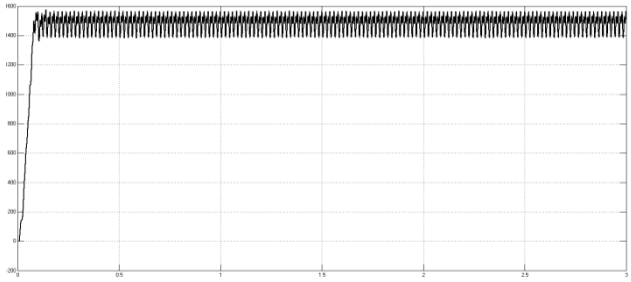


Figure 22: Speed Characteristics of Induction Fed Motor by 25 Level Inverter

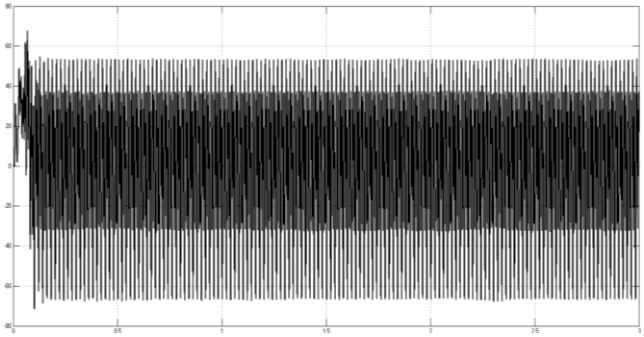


Figure 23: Torque Characteristics of Induction Fed Motor by 25 Level Inverter

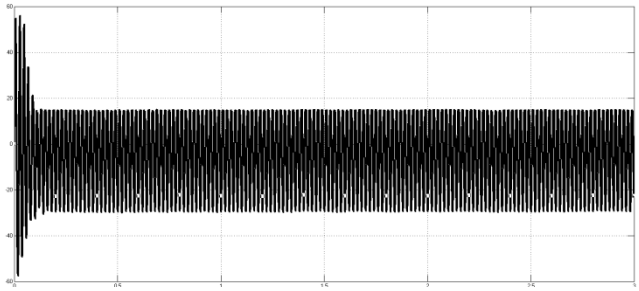


Figure 24: Stator Currents of Induction Fed Motor by 25 Level Inverter

As above Figure 22, 23, 24, shows the Speed, Electromagnetic Torque, and Stator Current of Proposed 25 level Inverter Fed Induction Motor Drive.

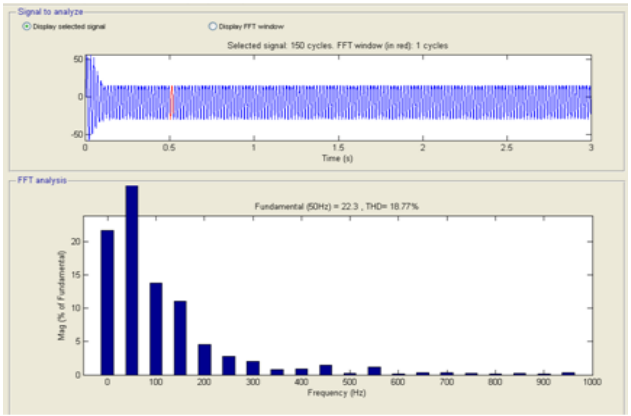


Figure 25: FFT Analysis of Stator Currents of Induction Fed Motor by 25 Level Inverter

Figure 25 shows the FFT analysis of Stator currents of Induction fed motor by 25 Level Inverter, here we get 18.72%.

Case 3: Proposed 35 level Multilevel Inverter Applied to Induction Machine Drive.

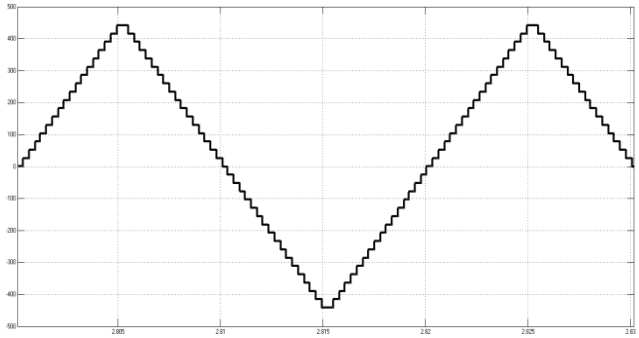


Figure 26: Output Voltage Wave form of 35 Level Inverter

Figure 26 shows the Output Voltage of Proposed 35 level Multilevel Inverter Applied to Induction Machine Drive.

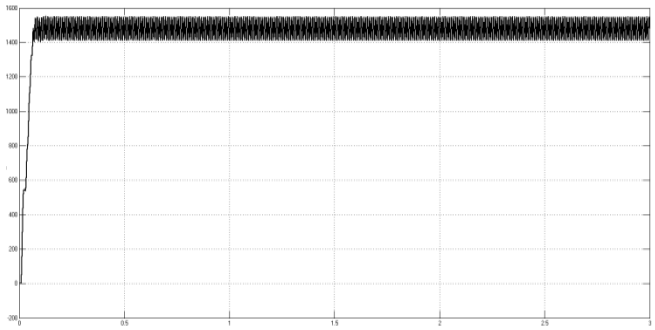


Figure 27: Speed Characteristics of Induction Fed Motor by 35 Level Inverter

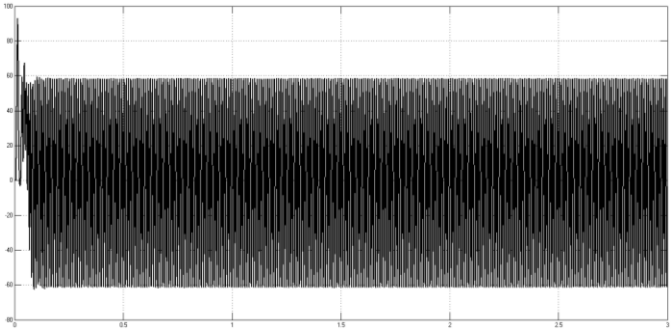


Figure 28: Torque Characteristics of Induction Fed Motor by 35 Level Inverter

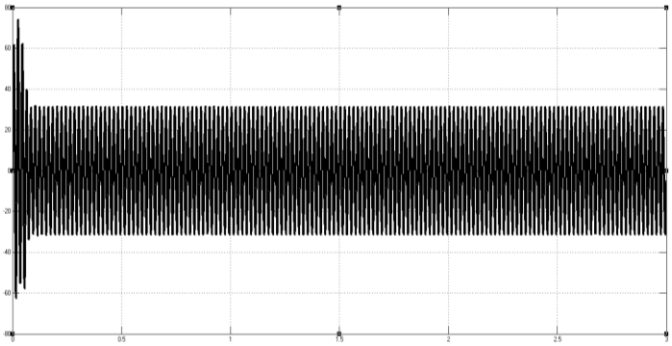


Figure 29: Stator Currents of Induction Fed Motor by 35 Level Inverter

As above Figure 27, 28, 29 shows the Speed, Electromagnetic Torque, and Stator Current of Proposed 35 level Inverter Fed Induction Motor Drive.

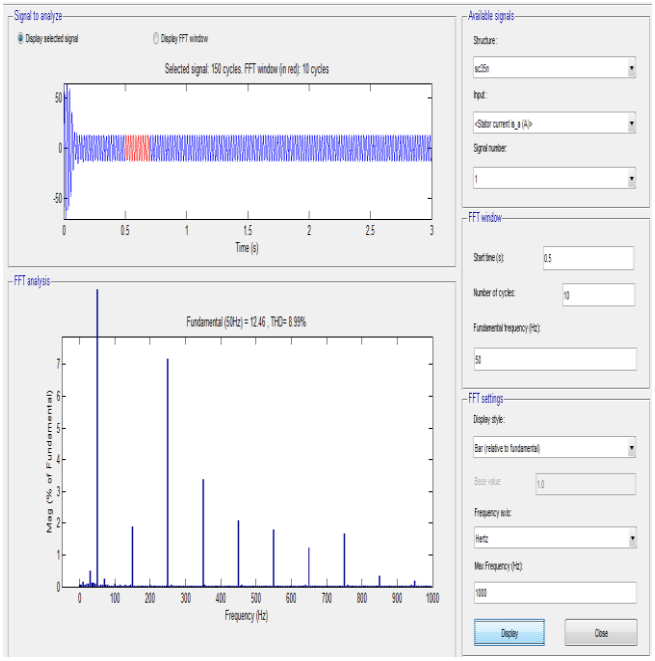


Figure 30: FFT Analysis of Stator Currents of Induction Fed Motor by 35 Level Inverter

Figure 30 shows the FFT analysis of Stator currents of Induction fed motor by 35 Level Inverter, here we get 8.99%.

CONCLUSIONS

From the above work done on the different levels of inverter structures of the proposed topology it is concluded that as the number of level of the inverter is being increased the structure of the output waveform is increased. Inspite of the improvement in the output voltage waveform the results obtained from the motor gave surprising results. The stator currents of the motor which must be sinusoidal are approaching near to a sine wave as the number of level is increasing. A comparative analysis on THD (total harmonic distortion) is done and for a thirteen level fed motor it is 24% and for a 25 level fed motor it is 18% and for 35 level motor it is 8.99%.One thing to be remembered is even though the levels are increased the inverter structure is not being changed and it remains as same and this the advantage of the proposed structure which can produce multiple outputs.

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